Patent claims

1. System (10) comprising at least two units (1, 2) with clock functionality, the units being coupled to a common system clock line (SCLK), a common internal clock line (ICLK), and a logic bus (L-BUS), whereby one sole unit (1, 2) is being dedicated as a master unit at a time,

the dedication of master unit (1, 2) being dependent on at least a signal being given so as not to select a given unit (1, 2) for being a master unit, and if a given unit (1, 2) is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit,

each unit (1, 2) comprising

-a clock source (CLK1, CLK2) for generating a clock source signal (CLK10, CLK20), the clock source signal being adapted for being output on the internal clock line (ICLK), and

-a phase lock loop device (P1, P2) generating a signal, which is derived from the signal on the internal clock line (ICLK), and which is output on the system clock line (S-CLK) if the unit is dedicated as master unit,

whereby one source clock signal (CLK10, CLK20) of a unit is output on the internal clock line (ICLK) and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices (CLKP1, CLKP2) being in phase with one another such that switchover from one phase lock loop output signal to another is seamless.

2. System according to claim 1, whereby the unit dedicated as master unit generates the clock source signal on the internal clock line (ICLK).

3. System according to claim 1 - 2, wherein each unit furthermore comprises

- a logic section (MS) communicating with the logic bus (L-BUS),

- a first bi-directional port (BD11; BD21) communicating with the internal clock line (ICLK),

- a second bi-directional port (BD12; BD22) communicating with a system clock line (SCLK),

the logic section (MS) of the unit controlling the first and second bi-directional ports (BD11, BD12, BD21, BD22) to input or output respective system clock signals (SCLK) and respective internal clock signals (ICLK) via enable signals (BD11E, BD12E, BD21E, BD22E).

4. System according to claim 3, whereby the enable signals are first changing state when the system clock (SCLK) is in a logic state with a certain predetermined security time interval from state changes of the system clock.

5. System according to claim 3 or 4, whereby the logic section (MS), in co-operation with other logic sections of other units, negotiate a priority scheme according to which a predetermined order for dedicating units is determined.

6. System according to any preceding claim, wherein the logic section of any unit comprises fault sense circuitry and whereby if a fault is detected in any device the system initiates switchover from a dedicated unit to a subsequent dedicated unit.

7. System according to any preceding claim, comprising an additional board (6, 7) not comprising any clock generating or clock evaluating functionality, the additional board being coupled to the system clock line (SCLK) but not to the internal clock line (ICLK) nor to the logic bus (L-BUS).

8. Unit (1, 2) comprising

-a logic section (MS) communicating with a logic bus (L-BUS),

-a clock source (CLK1, CLK2) for generating a clock source signal (CLK10, CLK20), the clock source signal being adapted for being output on an internal clock line (ICLK), and

-a phase lock loop device (P1, P2) having a predetermined characteristic and generating a signal (CLKP1), which is derived from a signal on an internal clock line (ICLK),

-first means (BD11; BD21) for outputting the clock source signal to the internal clock line (ICLK) or inputting the internal clock signal from the internal clock line,

-second means (BD12; BD22) for outputting the signal from the phase lock loop device to a system clock line (SCLK) or inputting the system clock signal,

the logic section (MS) of the unit controlling the first and second means (BD11, BD12, BD21, BD22) to input or output respective system clock signals (SCLK) and respective internal clock signals (ICLK), whereby

if the unit is dedicated as master unit, the logic section (MS) controls the phase lock loop generated signal derived from the internal clock signal to be output on the system clock line.

9. Unit according to claim 8, wherein if the unit is dedicated as master unit, the logic section (MS) controls the source clock signal (CLK10, CLK20) to be output on the internal clock line (ICLK).

10. Unit according to claim 8 or 9, wherein if the unit is not dedicated as master unit, the logic section (MS) controls the second means to input the system clock signal from the system clock line (SCLK).